MEAD Education S.A.

PLLs: Advanced Techniques

EPFL, LAUSANNE, SWITZERLAND
JUNE 23-27, 2014

MONDAY, June 23

8:30-12:00 am	PLL Fundamentals	Behzad Razavi
1:30-3:00 pm	High Speed Prescalers	Michiel Steyaert
3:30-5:00 pm	Low-Phase-Noise GHz VCO's in CMOS	Michiel Steyaert

TUESDAY, June 24

8:30-10:00 am	Single Chip CMOS Synthesizers for RF	Michiel Steyaert
10:30-12:00 am	Jitter and Phase Noise in PLLs	Ali Hajimiri
1:30-5:00 pm	VCO design	Ali Hajimiri

WEDNESDAY, June 25

8:30-12:00 am	Fractional-N PLLs for Frequency Synthesis	Ian Galton
1:30-3:00 pm	Fundamentals of All-Digital PLLs	Behzad Razavi
3:30-5:00 pm	Digitally-Controlled Oscillators	Behzad Razavi

THURSDAY, June 26

8:30-10:00 am	All-Digital PLL Architecture and Implementation for RF	Bogdan Staszewski
10:30-12:00 am	Digitally-Controlled Oscillator (DCO): System View	Bogdan Staszewski
1:30-3:00 pm	Time-to-Digital Converter (TDC)	Bogdan Staszewski
3:30-5:00 pm	Case Study of a Wide Operating Range DPLL with Bandwidth Tracking	Pavan Hanumolu

FRIDAY, June 27

8:30-10:00 am	Supply Noise Mitigation Techniques in PLLs	Pavan Hanumolu
10:30-12:00 am	Digital Multiplying Delay-Locked Loops	Pavan Hanumolu
1:30-3:00 pm	Digital Clock and Data Recovery Circuits	Pavan Hanumolu

PROGRAM

Monday, June 23rd 2014

8h30-12h00 am

PLL Fundamentals *(Behzad Razavi)*

This presentation introduces the basic phase-locked loop and its static and dynamic properties. Following a brief description of type-I PLLs, we focus on type-II PLLs and their realization using phase/frequency detectors and charge pumps. We derive simple equations for predicting the dynamic behavior of the loop. We also deal with various loop imperfections arising from the PFD and the charge pump and present circuit techniques that alleviate these issues. We finally provide a procedure for PLL design and discuss phase noise in PLLs.

1h30-3h00 pm

High Speed Prescalers *(Michiel Steyaert)*

High-speed CMOS prescaler, dual modulus prescaler and advanced circuit techniques, such as phase switching architectures, are discussed in detail. The limitations and requirements of the phase detector and loop filter towards fully integrated PLL synthesizers are discussed.

3h30-5h00 pm

Low-Phase-Noise GHz VCO's in CMOS *(Michiel Steyaert)*

Fundamentals and principles of VCO circuits. Relationship and link circuit design and phase noise. CMOS design strategies towards low phase noise. Lay-out and design issues of spiral inductors. Design examples of fully integrated VCO circuits in CMOS technologies.

Tuesday, June 24th 2014

8h30-10h00 am

Single Chip CMOS Synthesizers for RF *(Michiel Steyaert)*

Analysis and integration of varactors for CMOS VCO circuits. Effect of the varactors on phase noise. Effect of loop filter, phase detector (and dead-zone) and VCO noise on phase noise behavior of (fractional-N) PLL synthesizers. Design examples of fully integrated synthesizers in CMOS technologies.

10h30-12h00 am

Jitter and Phase Noise in PLLs *(Ali Hajimiri)*

We will discuss the time- and frequency-domain properties of phase locked loops. We will perform a parallel analysis of the jitter and phase noise properties of PLLs and discuss the impact of various building blocks on their properties and the output spectrum of PLLs. We will start our analysis with the discussion of first order loops and extend it to higher order loops.

1h30-5h00 pm

VCO Design *(Ali Hajimiri)*

In this module we will discuss modeling of phase noise in VCOs. We will start by introducing the time-varying response of oscillators and using the impulse sensitivity functions describe various noise conversion mechanisms in oscillators. In particular we should how low frequency noise and correlated and uncorrelated supply and substrate noise can convert to phase noise and how the time varying properties of oscillators can be exploited in oscillator design. Finally, we will show several practical examples of oscillators.

Wednesday, June 25th 2014

8h30-12h00 am

Fractional-N PLLs for Frequency Synthesis *(Ian Galton)*

This lecture explains the extension of integer-N PLLs to fractional-N PLLs for both fine tuning resolution and in-loop VCO modulation. It presents an overview of modulus quantization noise shaping techniques, tradeoffs associated with quantization noise shaping order and PLL loop bandwidth, non-ideal effects of particular concern in fractional-N PLLs such as charge pump nonlinearities and data-dependent multi-modulus divider delays, techniques for increasing loop bandwidth, simulation techniques, and case studies of example circuits and applications.

1h30-3h00 pm

Fundamentals of All-Digital PLLs *(Behzad Razavi)*

ADPLLs have recently become popular as they offer certain advantages over their analog counterparts. While the term "all-digital" is a misnomer, ADPLLs do simplify certain aspects of the design. This presentation describes the evolution from the analog PLLs to ADPLLs, identifying the DCO and the time-to-digital converter (TDC) as the design bottlenecks. Various TDC topologies are studied and the effect of TDC quantization is formulated. We also present several state-of-the-art examples, including TDC-less architectures.

3h30-5h00 pm

Digitally-Controlled Oscillators *(Behzad Razavi)*

DCOs are an integral component in all-digital PLLs, posing interesting and difficult challenges in the design. This presentation begins by introducing DCO performance parameters and describes basic DCO topologies. We then deal with tuning and resolution issues and view the DCO as a digital-to-frequency converter. Next, we study digital control of ring oscillators and LC oscillators, emphasizing the degradation in the performance and the increase in the complexity as higher resolutions are sought. We also present state-of-the-art examples.

Thursday, June 26th 2014

8h30-10h00 am

All-Digital PLL Architecture and Implementation for RF *(Bogdan Staszewski)*

The past several years has seen proliferation of all-digital phase-locked loops (ADPLL) for RF and high-performance frequency synthesis due to their clear benefits of flexibility, reconfigurability, transfer function precision, settling speed, frequency modulation capability, and amenability to integration with digital baseband and application processors. When implemented in nanoscale CMOS, the ADPLL also exhibits advantages of better performance, lower power consumption, lower area and cost over the traditional analog-intensive charge-pump PLL. In a typical ADPLL, a traditional VCO got directly replaced by a digitally controlled oscillator (DCO) for generating an output variable clock, a traditional phase/frequency detector and a charge pump got replaced by a time-to-digital converter (TDC) for detecting phase departures of the variable clock versus the frequency reference (FREF) clock, and an analog loop RC filter got replaced with a digital loop filter. The conversion gains of the DCO and TDC circuits are readily estimated and compensated using ”free” but powerful digital logic. This lecture presents a system level view of the ADPLL:

1. Principles of phase-domain frequency synthesis
2. ADPLL closed-loop behavior
3. Direct frequency modulation of ADPLL
4. Alternative TX architectures using ADPLL and PA regulator
5. Survey of published ADPLL architectures; TDC-less ADPLL; cell-based ADPLL design

10h30-12h00 am

Digitally-Controlled Oscillator (DCO): System View *(Bogdan Staszewski)*

A digitally controlled oscillator (DCO) lies at the heart of an all-digital phase-locked loop (ADPLL). It is based on an LC-tank with a negative resistance to perpetuate the oscillation— just like the traditional VCO, but with a significant difference in one of the components: instead of continuously tuned varactor (variable capacitor), the DCO now uses a large number of binary-controlled varactors. Each varactor can be placed in either high or low capacitive state. The composite varactor performs digital-to-capacitance conversion. This lecture presents a system level view of DCO.

1h30-3h00 pm

Time-to-Digital Converter (TDC) *(Bogdan Staszewski)*

A time-to-digital converter (TDC) is used in the ADPLL to perform the phase detection. It generates a digital variable phase or timestamps of the FREF edges in the units of the DCO clock period. The variable phase is a fixed-point digital word in which the fractional part is measured with a resolution of an inverter delay (about 10 ps in 40-nm CMOS). This lecture presents a system level view of TDC as well as its circuit-level implementation issues.

3h30-5h00 pm

Case Study of a Wide Operating Range DPLL with Bandwidth Tracking *(Pavan Hanumolu)*

This presentation discusses the design of a DPLL that employs a linear proportional path, a double integral path, bandwidth and tuning range tracking, and a novel delta-sigma digital to analog converter to achieve low jitter, wide operating range and low power.

Friday, June 27th 2014

8h30-10h00 am

Supply Noise Mitigation Techniques in PLLs *(Pavan Hanumolu)*

Supply noise affects the jitter performance of both analog and digital PLLs alike. This tutorial discusses several techniques to improve the supply noise immunity of PLLs. Design details of high supply-noise rejection regulators and novel PLL architectures will be discussed. Case study of several state-of-the-art supply-regulated PLLs will be presented.

10h30-12h00 am

Digital Multiplying Delay-Locked Loops *(Pavan Hanumolu)*

Digital multiplying delay-locked loops (DMDLLs) offer many advantages over their DPLL counterparts. This tutorial elucidates DMDLL benefits and discusses circuit implementation details. Case study of a state-of-the-art low power low jitter DMDLL will be presented.

1h30-3h00 pm

Digital Clock and Data Recovery Circuits *(Pavan Hanumolu)*

Digital clock and recovery circuits (CDRs) have recently emerged as an alternative to their more classical analog counterparts. This tutorial elucidates the design challenges and trade-offs involved in the design of digital CDRs. The jitter performance metrics such as jitter generation, jitter transfer, and jitter tolerance are related to digital CDR parameters and design guidelines will be provided. Design examples of state-of-the digital CDRs will be discussed.