MEAD Education S.A.

PLLs: Advanced Techniques

EPFL, LAUSANNE, SWITZERLAND
JUNE 22-26, 2015

MONDAY, June 22

8:30-12:00 am	PLL Fundamentals	Behzad Razavi
1:30-3:00 pm	High Speed Prescalers	Michiel Steyaert
3:30-5:00 pm	Low-Phase-Noise GHz VCO's in CMOS	Michiel Steyaert

TUESDAY, June 23

8:30-10:00 am	Single Chip CMOS Synthesizers for RF	Michiel Steyaert
10:30-12:00 am	VCO design	Ali Hajimiri
1:30-5:00 pm	Jitter and Phase Noise in PLLs	Ali Hajimiri

WEDNESDAY, June 24

8:30-12:00 am	Fractional-N PLLs for Frequency Synthesis	Ian Galton
1:30-3:00 pm	Fundamentals of All-Digital PLLs	Behzad Razavi
3:30-5:00 pm	Digitally-Controlled Oscillators	Behzad Razavi

THURSDAY, June 25

8:30-10:00 am	All-Digital PLL Architecture and Implementation for RF	Bogdan Staszewski
10:30-12:00 am	Digitally-Controlled Oscillator (DCO): System View	Bogdan Staszewski
1:30-3:00 pm	Time-to-Digital Converter (TDC)	Bogdan Staszewski
3:30-5:00 pm	Case Study of a Wide Operating Range DPLL with Bandwidth Tracking	Pavan Hanumolu

FRIDAY, June 26

8:30-10:00 am	Supply Noise Mitigation Techniques in PLLs	Pavan Hanumolu
10:30-12:00 am	Digital Multiplying Delay-Locked Loops	Pavan Hanumolu
1:30-3:00 pm	Digital Clock and Data Recovery Circuits	Pavan Hanumolu