PLLs Design

EPFL, LAUSANNE, SWITZERLAND
JUNE 22-26, 2020

MONDAY, June 22

8:30-10:00 am	Fundamentals of Analog PLLs	Michiel Steyaert
10:30-12:00 pm	Interference Effects in PLLs	Michiel Steyaert
1:30-5:00 pm	Spiral Inductor Interference, Deadzone and Phase Noise	Michiel Steyaert

TUESDAY, June 23

8:30-12:00 pm	All-Digital PLL Architecture and Implementation	Bogdan Staszewski
1:30-3:00 pm	Digitally Controlled Oscillator (DCO)	Bogdan Staszewski
3:30-5:00 pm	Time-to-Digital Converter (TDC)	Bogdan Staszewski

WEDNESDAY, June 24

8:30-12:00 pm	Design Techniques for Low Spur PLLs	Mike Shuo-Wei Chen
1:30-5:00 pm	VCO Design	Ali Hajimiri

THURSDAY, June 25

8:30-10:00 am	VCO Design	Ali Hajimiri
10:30-12:00pm & 1:30-5:00 pm	Jitter and Phase Noise in PLLs	Ali Hajimiri

FRIDAY, June 26

8:30-12:00 pm	Fractional N-PLLs for Frequency Synthesis	Ian Galton
1:30-3:00 pm	FDC-Based Digital PLLs	Ian Galton