Practical Aspects in Mixed-Signal ICs

EPFL, LAUSANNE, SWITZERLAND
AUGUST 31 – SEPTEMBER 4, 2020

MONDAY, August 31

8:30-10:00 am	The Analog and Digital Trade-off - The Impact of Technology Scaling	Jan Rabaey
10:30-12:00 pm & 1:30 -5:00 pm	Ultra Low-Power Mixed-Signal Interfaces for IoT and Biomedical Interfaces	Jan Rabaey

TUESDAY, September 1

8:30-12:00 pm	Noise Coupling in Mixed-Mode ICs: Mechanisms, Simulation, Measurement	Tim Schmerbeck
1:30-3:00 pm	Noise Coupling in Mixed-Mode ICs: Design Strategy/Hardware Example	Tim Schmerbeck
3:30-5:00 pm	Design for Electrostatic Discharge (ESD) Robustness in Silicon Integrated Circuits	Tim Schmerbeck

WEDNESDAY, September 2

8:30-10:00 am	Noise Calculation and Simulation in SC & CT Circuits	Christian Enz
10:30-12:00 pm	Noise and Offset Reduction Techniques	Christian Enz
1:30-3:00 pm	Offset and CMRR: Random and Systematic	Willy Sansen
3:30-5:00 pm	Fully-Differential Amplifiers	Willy Sansen

THURSDAY, September 3

8:30-12:00 pm	Matching Impairments in Mixed-Mode ICs	Herman Casier
1:30-3:00 pm	Practical Techniques of Frequency Compensation	Vadim Ivanov
3:30-5:00 pm	Circuit Techniques for OpAmp Speed and Accuracy	Vadim Ivanov

FRIDAY, September 4

8:30-10:00 am	Modeling and Simulation of Mixed-Mode Circuits	Pavan Hanumolu
10:30-12:00 pm	Interference Effects: CMRR/PSRR	Michiel Steyaert
1:30-3:00 pm	Design for EMC	Michiel Steyaert