Wireline SERDES Transceivers

UNIVERSITY OF SANTA CRUZ, CALIFORNIA
March 23-27, 2020

MONDAY, March 23

8:30 - 10:00 am	Introduction to Wireline Transceivers	Pavan Hanumolu
10:30 - 12:00 am	Transmitters (CML/VM)	Pavan Hanumolu
1:30 - 3:00 pm	FIR Equalizers (Tx/Rx)	Pavan Hanumolu
3:30 - 5:00 pm	Receivers (CTLE, DFE, Adaptation)	Pavan Hanumolu

TUESDAY, March 24

8:30 - 10:00 am	Phase-Locked Loops	Pavan Hanumolu
10:30 - 12:00 am	Advanced PLLs	Pavan Hanumolu
1:30 - 5:00 pm	Clock and Data Recovery	Pavan Hanumolu

WEDNESDAY, March 25

8:30 - 10:00 am	Advanced Signaling Methods	Armin Tajalli
10:30 - 12:00 am	Short Reach Transceiver Design Tradeoffs	Armin Tajalli
1:30 - 3:00 pm	Tradeoffs in Slicer Design	Armin Tajalli

THURSDAY, March 26

8:30 - 10:00 am	Clock and Data Recovery (ct'd)	Pavan Hanumolu
10:30 - 12:00 am	Baud-Rate CDRs	Pavan Hanumolu
1:30 - 3:00 pm	Introduction to PAM4 Signaling	Pavan Hanumolu
3:00 - 5:00 pm	Trans-Impedance Amplifiers	Pavan Hanumolu

FRIDAY, March 27

8:30 - 10:00 am	Optical Transmitters	Sam Palermo
10:30 - 12:00 am	Design of ADC-Based Serial Links	Sam Palermo