



## PLLs and Clock Recovery

EPFL PREMISES, LAUSANNE, SWITZERLAND  
JUNE 28 - JULY 1, 2010

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### MONDAY, JUNE 28

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8:30 - 10:00 am	Basic Concepts of PLL Topologies	Michiel Steyaert
10:30 - 12:00 am	CMOS Prescalers & Advanced Loop Filters	Michiel Steyaert
1:30 - 5:00 pm	Integrated VCOs and Synthesizers	Michiel Steyaert

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### TUESDAY, JUNE 29

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8:30 - 12:00 am	Modeling and Design of High-Speed VCOs	Ali Hajimiri
1:30 - 3:00 pm	Jitter and Phase Noise in PLLs	Ali Hajimiri
3:30 - 5:00 pm	Low-Power Crystal Oscillators	Michiel Steyaert

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### WEDNESDAY, JUNE 30

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8:30 - 12:00 am	High Speed Synthesizers for Communications	John Cowles
1:30 - 5:00 pm	Fractional-N PLLs for Frequency Synthesis	Ian Galton

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### THURSDAY, JULY 1

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8:30 - 12:00 am & 1:30 - 5:00 pm	Clock and Data Recovery	Lawrence DeVito
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