

Practical Aspects in Mixed-Signal ICs

**EPFL PREMISES, LAUSANNE, SWITZERLAND
AUGUST 23-27, 2010**

MONDAY, AUGUST 23

8:30 - 10:00 am	Trade-off between Analog and Digital - The Impact of Technology Scaling	Jan Rabaey
10:30 - 12:00 am	Ultra Low-Power Mixed Signal Interfaces	Jan Rabaey
1:30 - 5:00 pm	Noise Coupling in Mixed-Mode ICs: Mechanisms	Tim Schmerbeck

TUESDAY, AUGUST 24

8:30 - 10:00 am	Noise Coupling in Mixed-Mode ICs: Simulation/Measurement	Tim Schmerbeck
10:30 - 12:00 am	Noise Coupling in Mixed-Mode ICs: Design Strategy/Hardware Example	Tim Schmerbeck
1:30 - 5:00 pm	Matching Impairments in Mixed-Mode ICs	Herman Casier

WEDNESDAY, AUGUST 25

8:30 - 10:00 am	Interference Effects: CMRR/PSRR	Michiel Steyaert
10:30 - 12:00 am	Opamp Design Towards Max. GBW PSRR	Michiel Steyaert
1:30 - 3:00 pm	Design for EMC	Michiel Steyaert
3:30 - 5:00 pm	Ultra-Low Voltage Analog Circuits	Christian Enz

THURSDAY, AUGUST 26

8:30 - 10:00 am	Offset and CMRR: Random and Systematic	Willy Sansen
10:30 - 12:00 am	Fully-Differential Amplifiers	Willy Sansen
1:30 - 5:00 pm	Sampled Noise in SC Circuits	Gabor Temes

FRIDAY, AUGUST 27

8:30 - 12:00 am	Design for Manufacturing Robustness	Barrie Gilbert
1:30 - 5:00 pm	High-Voltage / High-Field Problems	Yusuf Leblebici
