# SERDES Design for Wireline and Optical Communications

## UNIVERSITY OF SANTA CRUZ, CALIFORNIA
## March 25-28, 2019

### MONDAY, March 25

| | | |
|---|---|---|
| 8:30 - 10:00 am | Introduction to NRZ and PAM4 Transceivers | Behzad Razavi |
| 10:30 - 12:00 am | PLL Design for Transmitters and Receivers | Behzad Razavi |
| 1:30 - 3:00 pm | High-Performance VCO Design | Behzad Razavi |
| 3:30 - 5:00 pm | Multiplexer Design, Examples of the State of the Art | Behzad Razavi |

### TUESDAY, March 26

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|---|---|---|
| 8:30 - 10:00 am | Transistor-Level Design of Linear Continuous-Time Equalizers | Behzad Razavi |
| 10:30 - 12:00 am | Transistor-Level Design of Decision-Feedback Equalizers | Behzad Razavi |
| 1:30 - 3:00 pm | Demultiplexers | Behzad Razavi |
| 3:30 - 5:00 pm | Examples of State of the Art | Behzad Razavi |

### WEDNESDAY, March 27

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|---|---|---|
| 8:30 - 10:00 am | Analog Clock and Date Recovery Circuits | Behzad Razavi |
| 10:30 - 12:00 am | Digital Clock and Date Recovery Circuits | Behzad Razavi |
| 1:30 - 5:00 pm | Studies | Behzad Razavi |

### THURSDAY, March 28

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|---|---|---|
| 8:30 - 10:00 am | Advance Signaling Methods and Circuits for High Speed Serial Data Communications | Armin Tajalli |
| 10:30 - 12:00 am | Short Reach Transceiver Design Tradeoffs | Armin Tajalli |
| 1:30 - 3:00 pm | Slicer Design | Armin Tajalli |