



Transistor-Level Analog IC Design

**EPFL PREMISES, LAUSANNE, SWITZERLAND
JUNE 21-23, 2010**

MONDAY, JUNE 21

8:30 - 10:00 am	Introduction & MOS Transistors	Klaas Bult
10:30 - 12:00 am	Single-Stage Amplifiers, part I	Klaas Bult
1:30 - 3:00 pm	Single-Stage Amplifiers, part II	Klaas Bult
3:30 - 5:00 pm	gm/Id Methodology for MOS Device Sizing	Maher Kayal

TUESDAY, JUNE 22

8:30 - 10:00 am	Noise in MOS Transistors	Klaas Bult
10:30 - 12:00 am	Distortion	Klaas Bult
1:30 - 3:00 pm	Basic Sub-Circuits	Klaas Bult
3:30 - 5:00 pm	Basic Analog Structures Design	Maher Kayal

WEDNESDAY, JUNE 23

8:30 - 10:00 am	Gain-Boosting and Settling Behavior	Klaas Bult
10:30 - 12:00 am	Two-Stage Amplifiers	Klaas Bult
1:30 - 5:00 pm	Matching of MOS Transistors in Deep-Submicron	Marcel Pelgrom
