

Transistor-Level Analog Design: Theory and Hands-on

EPFL, LAUSANNE, SWITZERLAND JUNE 23-27, 2014

JUNE 23-27, 2014 MONDAY, June 23		
10:30-12:00 am	Single-Stage OpAmps	Klaas Bult
1:30-3:00 pm	Single-Stage OpAmps	Klaas Bult
3:30-5:00 pm	Noise in MOS Transistors	Klaas Bult
TUESDAY, Ju	ne 24	
8:30-10:00 am	Distortion	Klaas Bult
10:30-12:00 am	Opamp Towards Maximum GBW	Michiel Steyaert
1:30-5:00 pm	Matching of MOS Transistors in Deep-Submicron	Marcel Pelgrom
WEDNESDAY	, June 25	
8:30-10:00 am	Basic Sub-Circuits	Klaas Bult
10:30-12:00 am	Gain-Boosting & Settling Behaviour	Klaas Bult
1:30-5:00 pm	Layout Considerations in Mixed-Signal IC Design	Marcel Pelgrom
THURSDAY, J	lune 26	
8:30-10:00 am	Two-Stage Amplifiers	Klaas Bult
10:30-12:00 am	Digitally-Assisted Analog Circuits	Marc Pastre
1:30-3:00 pm	MOS Device Sizing	Maher Kayal
3:30-5:00 pm	LAB SESSION: Basic OTA Design	Maher Kayal + assistants
FRIDAY, June	27	
8:30-10:00 am	Folded Cascode Design & Offset Compensation	Maher Kayal
10:30-12:00 am	LAB SESSION: Folded Cascode design	Maher Kayal + assistants
1:30-3:00 pm	LAB SESSION: Offset reduction design	Maher Kayal + assistants