MEAD Education S.A.

# Transistor-Level Analog Design:
## Theory and Hands-on

### MEAD-EPFL, LAUSANNE, SWITZERLAND
### JUNE 22-26, 2015

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## MONDAY, June 22

| | | |
|---|---|---|
| 8:30-10:00 am | Introduction & MOS Transistors | Klaas Bult |
| 10:30-12:00 am | Single-Stage OpAmps, Part 1 | Klaas Bult |
| 1:30-3:00 pm | Single-Stage OpAmps, Part 2 | Klaas Bult |
| 1:30-3:00 pm | Noise in MOS Transistors | Klaas Bult |

## TUESDAY, June 23

| | | |
|---|---|---|
| 8:30-10:00 am | Distortion | Klaas Bult |
| 10:30-12:00 am | Basic Sub-Circuits | Klaas Bult |
| 1:30-5:00 pm | Matching of MOS Transistors in Deep-Submicron | Marcel Pelgrom |

## WEDNESDAY, June 24

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|---|---|---|
| 8:30-10:00 am | Gain-Boosting & Settling Behavior | Klaas Bult |
| 10:30-12:00 am | Two-Stage Amplifiers | Klaas Bult |
| 1:30-5:00 pm | Layout Considerations in Mixed-Signal Circuit Design | Marcel Pelgrom |

## THURSDAY, June 25

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|---|---|---|
| 8:30-10:00 am | MOS Device Sizing | Maher Kayal |
| 10:30-12:00 am | OTAs Procedural Sizing | Maher Kayal |
| 1:30-5:00 pm | LAB SESSION: Basic OTA design | Maher Kayal+ assistants |

## FRIDAY, June 26

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|---|---|---|
| 8:30-10:00 am | Digitally-Assisted Offset Compensation | Maher Kayal |
| 10:30-12:00 am | LAB SESSION: Folded Cascode design | Maher Kayal+ assistants |
| 1:30-3:00 pm | LAB SESSION: Offset reduction design | Maher Kayal+ assistants |