PRACTICAL DESIGN OF DATA CONVERTERS

ON-LINE CLASS by MS TEAMS

February 28 - March 11, 2022

WEEK 1	**FEB 18 - MAR 4, 2022**
WEEK 2	**MAR 7-11, 2022**

	Central European Time	Eastern Standard Time	Pacific Standard Time	India Standard Time
DAILY	**CET (Lausanne)**	**EST (New York)**	**PST (California)**	**IST (India)**
Module 1	3:00-4:30 pm	9:00-10:30 am	6:00-7:30 am	7:30-9:00 pm
Module 2	5:00-6:30 pm	11:00-12:30 am	8:00-9:30 am	9:30-11:00 pm
Module 3 (Tue March 8)	6:45-7:30 pm	12:45 am-1:30 pm	09:45-10:30 am	11:15-12:00 pm

WEEK 1	Module		
Monday, February 28	1	Basic ADC Topologies: Overview	Marcel Pelgrom
	2	Specifications Overview: INL, DNL, THD, SFDR, SNR, DR, ENOB, jitter	Marcel Pelgrom
Tuesday, March 1	1	Simulating ADCs: Frequency Domain: FFT, bin choice, windowing, noise level, kT/C noise	Shanthi Pavan
	2	Oversampling ADCs : Discrete-and-Continuous-time Delta-Sigma Converters	Shanthi Pavan
Wednesday, March 2	1	Limits of Nyquist ADC Architectures	Filip Tavernier
	2	ADCs Comparators	Marcel Pelgrom
Thursday, March 3	1	ADC Comparators and Reference	Marcel Pelgrom
	2	SAR versus Pipeline	Marcel Pelgrom
Friday, March 4	1&2	Time Interleaved ADCs	Marcel Pelgrom
WEEK 2			
Monday, March 7	1&2	Mismatch-Shaping Multi-bit DACs	Ian Galton
Tuesday, March 8	1	Case Study of a High-Speed Single-Channel SAR ADC	Filip Tavernier
	2	Case Study of a Time-Interleaved Hybrid ADC	Filip Tavernier
	3	Incremental Data Converters	Gabor Temes
Wednesday, March 9	1	Case study: Low-Power Data Converters (1)	Kofi Makinwa
	2	Case study: Low-Power Data Converters (2)	Kofi Makinwa
Thursday, March 10	1	Simulating Sigma-Delta Converters: Part 1	Shanthi Pavan
	2	Simulating Sigma-Delta Converters: Part 2	Shanthi Pavan
Friday, March 11	1	Case Study: Low-Speed Delta-Sigma Converter	Shanthi Pavan
	2	Case Study: High-Speed Delta-Sigma Converter	Shanthi Pavan