PRACTICAL DESIGN OF DATA CONVERTERS

ON-LINE CLASS on MS TEAMS

February 27 - March 10, 2023

WEEK 1	**FEB 27 - MARCH 3**
WEEK 2	**MARCH 6-10**

DAILY	Central European Time **CET (Lausanne)**	Eastern Standard Time **EST (New York)**	Pacific Standard Time **PST (California)**	India Standard Time **IST (India)**
Module 1	3:00-4:30 pm	9:00-10:30 am	6:00-7:30 am	6:30-8:00 pm
Module 2	5:00-6:30 pm	11:00-12:30 am	8:00-9:30 am	8:30-10:00pm
Module 3 (Tutorial, March 7)	6:45-7:30 pm	12:45-01:30 pm	09:45-10:30 am	10:45-11:30 pm

WEEK 1	*Module*		
Monday, February 27	1	Basic ADC Topologies: Overview	Marcel Pelgrom
	2	Specifications Overview: INL, DNL, THD, SFDR, SNR, DR, ENOB, Jitter	Marcel Pelgrom
Tuesday, February 28	1	Simulating ADCs: Frequency Domain: FFT, Bin Choice, Windowing, Noise Level, kT/C Noise	Shanthi Pavan
	2	Oversampling ADCs : Discrete-and-Continuous-time Delta-Sigma Converters	Shanthi Pavan
Wednesday, March 1	1	Limits of Nyquist ADC Architectures	Filip Tavernier
	2	ADC Comparators	Marcel Pelgrom
Thursday, March 2	1	ADC Comparators and Reference	Marcel Pelgrom
	2	SAR Versus Pipeline	Marcel Pelgrom
Friday, March 3	1&2	Time Interleaved ADCs	Marcel Pelgrom

WEEK 2	*Module*		
Monday, March 6	1&2	Mismatch-Shaping Multi-bit DACs	Ian Galton
Tuesday, March 7	1	Case Study of a High-Speed Single-Channel SAR ADC	Filip Tavernier
	2	Case Study of a Time-Interleaved Hybrid ADC	Filip Tavernier
	3	Incremental Data Converters	Gabor Temes
Wednesday, March 8	1	Case Study: Low-Power Data Converters (1)	Kofi Makinwa
	2	Case Study: Low-Power Data Converters (2)	Kofi Makinwa
Thursday, March 9	1	Simulating Sigma-Delta Converters: Part 1	Shanthi Pavan
	2	Simulating Sigma-Delta Converters: Part 2	Shanthi Pavan
Friday, March 10	1	Case Study: Low-Speed Delta Sigma Converter	Shanthi Pavan
	2	Case Study: High-Speed Delta Sigma Converter	Shanthi Pavan