PRACTICAL DESIGN OF DATA CONVERTERS

Live Course @ EPFL, Lausanne, Switzerland

JUNE 17-21, 2024

Monday, June 17		
08:30 - 10:00 am	Basic ADC Topologies: overview	Marcel Pelgrom
10:30 - 12:00 am	Specifications Overview: INL, DNL, THD, SFDR, SNR, DR, ENOB, jitter	Marcel Pelgrom
01:30 - 03:00 pm	ADC Comparators	Marcel Pelgrom
03:30 - 05:00 pm	SAR versus Pipeline	Marcel Pelgrom
Tuesday, June 18		
08:30 - 12:00 am	Time interleaved ADC	Marcel Pelgrom
01:30 - 03:00 pm	Limits of Nyquist ADC Architecture	Filip Tavernier
03:30 - 05:00 pm	Case Study of a High-Speed Single-Channel SAR ADC	Filip Tavernier
Wednesday, June 19		
08:30 - 10:00 am	Case Study of a Time-Interleaved Hybrid ADC	Filip Tavernier
10:30 - 12:00 am	Simulating ADCs: Frequency Domain: FFT, bin choice, windowing, noise level, kT/C noise	Shanthi Pavan
01:30 - 03:00 pm	Case study: low-power data Converters (1)	Kofi Makinwa
03:30 - 05:00 pm	Case study: low-power data Converters (2)	Kofi Makinwa
Thursday, June 20		
08:30 - 12:00 am	Current Steering DAC's	Klaas Bult
01:30 - 03:00 pm	Continuous-Time Pipeline ADC	Shanthi Pavan
03:30 - 05:00 pm	Oversampling ADCs : Discrete-and-Continuous-time Delta-Sigma Converters	Shanthi Pavan
Friday, June 21		
08:30 - 12:00 am	Mismatch-Shaping Multi-Bit DACs	Ian Galton
01:30 - 03:00 pm	Simulating Sigma-Delta Converters	Shanthi Pavan
03:30 - 05:00 pm	Case Study: High-Performance Delta Sigma Converter	Shanthi Pavan