



PLL Design

ON-LINE CLASS by Microsoft TEAMS

May 2-13, 2022

WEEK 1		MAY 2-6, 2022		
WEEK 2		MAY 9-13, 2022		
DAILY	Central European Time	Eastern Standard Time	Pacific Standard Time	India Standard Time
	CET (Lausanne)	EST (New York)	PST (California)	IST (India)
Module 1	3:00-4:30 pm	9:00-10:30 am	6:00-7:30 am	7:30-9:00 pm
Module 2	5:00-6:30 pm	11:00 -12:30 pm	8:00-9:30 am	9:30-11:0 0pm
WEEK 1	Module			
Monday, May 2	1	Fundamentals of Analog PLLs		Michiel Steyaert
	2	Interference Effects in PLL's		Michiel Steyaert
Tuesday, May 3	1&2	Spiral Inductor Interference, Deadzone and Phase Noise		Michiel Steyaert
Wednesday, May 4	1&2	Analog Fractional-N PLLs for Frequency Synthesis		Ian Galton
Thursday, May 5	1	PLL Analysis and Modeling		Sam Palermo
	2	PLL Building Blocks		Sam Palermo
Friday, May 6	1	Clock Generation and Distribution in Wireline Systems		Sam Palermo
	2	PLL-Based Clock and Data Recovery Systems		Sam Palermo
WEEK 2	Module			
Monday, May 9	1&2	VCO Design		Ali Hajimiri
Tuesday, May 10	1&2	Jitter and Phase Noise in PLLs		Ai Hajimiri
Wednesday, May 11	1&2	All-Digital PLL Architecture and Implementation		Bogdan Staszewski
Thursday, May 12	1	Digitally-Controlled Oscillator (DCO)		Bogdan Staszewski
	2	Time-to-Digital Converter (TDC)		Bogdan Staszewski
Friday, May 13	1	FDC-based Digital PLLs		Ian Galton