MEAD Education S.A.

Practical PLL Design for Frequency Synthesis and Clocking

EPFL, LAUSANNE, SWITZERLAND
JUNE 20-24, 2016

MONDAY, June 20

8:30-10:00 am	Basic Concepts of PLLs	Michiel Steyaert
10:30-12:00 am	VCO Design	Ali Hajimiri
1:30 -5:00 pm	Jitter and Phase Noise in PLLs	Ali Hajimiri

TUESDAY, June 21

8:30-10:00 am	Interference Effects in PLLs	Michiel Steyaert
10:30-12:00 am & 1:30-3:00 pm	Integrated VCOs and Synthesizers	Michiel Steyaert
3:30-5:00 pm	Crystal Oscillators	Michiel Steyaert

WEDNESDAY, June 22

8:30-12:00 am	Fractional N-PLLs for Frequency Synthesis	Ian Galton
1:30-5:00 pm	All-Digital PLL Architecture and Implementation	Bogdan Staszewski

THURSDAY, June 23

8:30-10:00 am	Digitally Controlled Oscillator (DCO)	Bogdan Staszewski
10:30-12:00 am	Time-to-Digital Converter (TDC)	Bogdan Staszewski
1:30-3:00 pm	FDC-Based Digital PLLs	Ian Galton
3:30-5:00 pm	Case Study of a Wide Operating Range DPLL with Bandwidth Tracking	Pavan Hanumolu

FRIDAY, June 24

8:30-10:00 am	Supply Noise Mitigation Techniques in PLLs	Pavan Hanumolu
10:30-12:00 am	Digital Multiplying Delay-Locked Loops	Pavan Hanumolu
1:30 - 3:00 pm	Injection-Locked Clock Multipliers	Pavan Hanumolu