

PLLs & Oscillators

EPFL, LAUSANNE, SWITZERLAND JUNE 17-21, 2019

MONDAY, June 17		
8:30-10:00 am	Fundamentals of Analog PLLs	Michiel Steyaert
10:30-12:00 am	Interference Effects in PLLs	Michiel Steyaert
1:30 -5:00 pm	Spiral Inductor Interference, Deadzone and Phase Noise	Michiel Steyaert
TUESDAY, Ju	ne 18	
8:30-12:00 am	VCO Design	Ali Hajimiri
1:30 -5:00 pm	Jitter and Phase Noise in PLLs	Ali Hajimiri
WEDNESDAY	, June 19	
8:30-12:00 am	All-Digital PLL Architecture and Implementation	Bogdan Staszewsk
1:30-3:00 pm	Digitally Controlled Oscillator (DCO)	Bogdan Staszewski
3:30-5:00 pm	Time-to-Digital Converter (TDC)	Bogdan Staszewsk
THURSDAY, J	lune 20	
8:30-12:00 am	PLL Imperfections	Behzad Razavi
1:30-3:00 pm	Wideband PLL Design Study	Behzad Razavi
3:30-5:00 pm	Delay-Locked Loops	Behzad Razavi
FRIDAY, June	21	
8:30-12:00 am	Analog Fractional N-PLLs for Frequency Synthesis	lan Galton
1:30-3:00 pm	FDC-Based Digital PLLs	lan Galton