# Wireline SERDES Transceivers

***ON-LINE CLASS by Microsoft TEAMS***

**June 7-18, 2021**

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|---|---|---|---|---|
| ***WEEK 1*** | **JUNE 7-11** | 8 Modules (1:30hr each), 2 Modules per day | | |
| ***WEEK 2*** | **JUNE 14-18** | 8 Modules (1:30hr each), 2 Modules per day | | |
| ***DAILY*** | Central European Time | Eastern Standard Time | Pacific Standard Time | India Standard Time |
| | **CET (Lausanne)** | **EST (New York)** | **PST (California)** | **IST (India)** |
| Module 1 | 3:00-4:30 pm | 9:00-10:30 am | 6:00-7:30 am | 6:30-8:00 pm |
| Module 2 | 5:00-6:30 pm | 11:00 -12:30 pm | 8:00-9:30 am | 8:30-10:00 pm |

| ***WEEK 1*** | Module | | |
|---|---|---|---|
| Monday, June 7 | 1 | Introduction to Wireline Transceivers | Pavan Hanumolu |
| | 2 | Transmitters (CML/VM) | Pavan Hanumolu |
| Tuesday, June 8 | 1 | FIR Equalizers (Tx/Rx) | Pavan Hanumolu |
| | 2 | Receivers (CTLE, DFE, Adaptation) | Pavan Hanumolu |
| Wednesday, June 9 | 1 | DFE, Adaptation | Pavan Hanumolu |
| | 2 | Phase-Locked Loops | Pavan Hanumolu |
| Thursday, June 10 | 1 | Advanced PLLs | Pavan Hanumolu |
| | 2 | Clock and Data Recovery | Pavan Hanumolu |
| Friday, June 11 | 1 | Phase/Frequency Detectors | Pavan Hanumolu |
| | 2 | Advanced CDRs | Pavan Hanumolu |

| ***WEEK 2*** | Module | | |
|---|---|---|---|
| Monday, June 14 | 1 | Baud-Rate CDRs | Pavan Hanumolu |
| | 2 | Trans-Impedance Amplifiers | Pavan Hanumolu |
| Tuesday, June 15 | 1 | Advanced Signaling Methods | Armin Tajalli |
| | 2 | Short Reach Transceiver Design Tradeoffs | Armin Tajalli |
| Wednesday, June 16 | 1 | Tradeoffs in Design of Slicers | Armin Tajalli |
| | 2 | Discrete-Time Front-End Design | Armin Tajalli |
| Thursday, June 17 | 1 | Optical Transmitters | Sam Palermo |
| | 2 | ADC-Based RX Analysis and Digital Equalization | Sam Palermo |
| Friday, June 18 | 1 | Wireline RX Time-Interleaved ADC Design and Calibration | Sam Palermo |
| | 2 | DSP-DAC Wireline Transmitters | Sam Palermo |
| | 0.5 | Course Evaluation, Survey Results | Vlado Valence, All |