



# Wireline SERDES Transceivers

**ON-LINE CLASS by Microsoft TEAMS**

**May 9-20, 2022**

| <b>WEEK 1</b>     |                       | <b>MAY 9-13, 2022</b>                                   |                         |                     |                |
|-------------------|-----------------------|---|-------------------------|---------------------|----------------|
| <b>WEEK 2</b>     |                       | <b>MAY 16-20, 2022</b>                                  |                         |                     |                |
| <b>DAILY</b>      | Central European Time | Eastern Standard Time                                   | Pacific Standard Time   | India Standard Time |                |
|                   | <b>CET (Lausanne)</b> | <b>EST (New York)</b>                                   | <b>PST (California)</b> | <b>IST (India)</b>  |                |
| Module 1          | 3:30-5:00 pm          | 9:30-11:00 am   | 6:30-8:00 am            | 8:00-9:30 pm        |                |
| Module 2          | 5:30-7:00 pm          | 11:30 -1:00 pm  | 8:30-10:00 am           | 10:00-11:30pm       |                |
| <b>WEEK 1</b>     | Module                |   |                         |                     |                |
| Monday, May 9     | 1                     | Introduction to Wireline Transceivers                   |                         |                     | Pavan Hanumolu |
|                   | 2                     | Transmitters (CML/VM)                                   |                         |                     | Pavan Hanumolu |
| Tuesday, May 10   | 1                     | FIR Equalizers (Tx/Rx)                                  |                         |                     | Pavan Hanumolu |
|                   | 2                     | CTLE  |                         |                     | Pavan Hanumolu |
| Wednesday, May 11 | 1                     | DFE, Adaptation   |                         |                     | Pavan Hanumolu |
|                   | 2                     | Phase-Locked Loops                                      |                         |                     | Pavan Hanumolu |
| Thursday, May 12  | 1                     | Advanced PLLs   |                         |                     | Pavan Hanumolu |
|                   | 2                     | Clock and Data Recovery                                 |                         |                     | Pavan Hanumolu |
| Friday, May 13    | 1                     | Phase/Frequency detectors                               |                         |                     | Pavan Hanumolu |
|                   | 2                     | Advanced CDRs   |                         |                     | Pavan Hanumolu |
| <b>WEEK 2</b>     | Module                |   |                         |                     |                |
| Monday, May 16    | 1                     | Baud-rate CDRs  |                         |                     | Pavan Hanumolu |
|                   | 2                     | Trans-Impedance Amplifiers                              |                         |                     | Pavan Hanumolu |
| Tuesday, May 17   | 1                     | Advanced Signaling Methods                              |                         |                     | Armin Tajalli  |
|                   | 2                     | Short Reach Transceiver Design Tradeoffs                |                         |                     | Armin Tajalli  |
| Wednesday, May 18 | 1                     | Tradeoffs in Design of Slicers                          |                         |                     | Armin Tajalli  |
|                   | 2                     | Discrete-Time Front-End Design                          |                         |                     | Armin Tajalli  |
| Thursday, May 19  | 1                     | Optical Transmitters                                    |                         |                     | Sam Palermo    |
|                   | 2                     | ADC-Based RX Analysis and Digital Equalization          |                         |                     | Sam Palermo    |
| Friday, May 20    | 1                     | Wireline RX Time-Interleaved ADC Design and Calibration |                         |                     | Sam Palermo    |
|                   | 2                     | DSP-DAC Wireline Transmitters                           |                         |                     | Sam Palermo    |