Wireline SERDES Transceivers

ON-LINE CLASS on Microsoft TEAMS

May 6-17, 2024

WEEK 1	**MAY 6-10, 2024**
WEEK 2	**MAY 13-17, 2024**

DAILY	Central European Time **CET (Lausanne)**	Eastern Standard Time **EST (New York)**	Pacific Standard Time **PST (California)**	India Standard Time **IST (India)**
Module 1	3:30-5:00 pm	09:30-11:00 am	6:30-8:00 am	7:00-8:30 pm
Module 2	5:30-7:00 pm	11:30 am-01:00 pm	8:30-10:00 am	9:00-10:30 pm

WEEK 1	***Module***		
Monday, May 6	1	Introduction to Wireline Transceivers	Pavan Hanumolu
	2	Transmitters (CML/VM)	Pavan Hanumolu
Tuesday, May 7	1	FIR Equalizers (Tx/Rx)	Pavan Hanumolu
	2	CTLE	Pavan Hanumolu
Wednesday, May 8	1	DFE, Adaptation	Pavan Hanumolu
	2	Phase-Locked Loops	Pavan Hanumolu
Thursday, May 9	1	Advanced PLLs	Pavan Hanumolu
	2	Clock and Data Recovery	Pavan Hanumolu
Friday, May 10	1	Phase/Frequency Detectors	Pavan Hanumolu
	2	Advanced CDRs	Pavan Hanumolu
WEEK 2	***Module***		
Monday, May 13	1	Baud-Rate CDRs	Pavan Hanumolu
	2	Trans-Impedance Amplifiers	Pavan Hanumolu
Tuesday, May 14	1	Advanced Signaling Methods	Armin Tajalli
	2	Short Reach Transceiver Design Tradeoffs	Armin Tajalli
Wednesday, May 15	1	Tradeoffs in Design of Slicers	Armin Tajalli
	2	Discrete-Time Front-End Design	Armin Tajalli
Thursday, May 16	1	Optical Transmitters	Sam Palermo
	2	ADC-Based RX Analysis and Digital Equalization	Sam Palermo
Friday, May 17	1	Wireline RX Time-Interleaved ADC Design and Calibration	Sam Palermo
	2	DSP-DAC Wireline Transmitters	Sam Palermo