Practical Aspects in Mixed-Signal ICs

EPFL, LAUSANNE, SWITZERLAND
AUGUST 28 – SEPTEMBER 1, 2017

MONDAY, August 28

8:30 - 10:00 am	Trade-off between Analog and Digital - The Impact of Technology Scaling	Jan Rabaey
10:30 - 12:00 am	Ultra Low-Power Mixed Signal Interfaces	Jan Rabaey
1:30 -5:00 pm	Noise Coupling in Mixed-Mode ICs: Mechanisms, Simulation, Measurement	Tim Schmerbeck

TUESDAY, August 29

8:30 - 12:00 am	Noise Coupling in Mixed-Mode ICs: Design Strategy/Hardware Example	Tim Schmerbeck
10:30 - 12:00 am	Design for Electrostatic Discharge (ESD) Robustness in Silicon Integrated Circuits	Tim Schmerbeck
1:30 - 5:00 pm	Digitally-Assisted Analog Circuits	Marc Pastre

WEDNESDAY, August 30

8:30 - 10:00 am	Offset and CMRR: Random and Systematic	Willy Sansen
10:30 - 12:00 am	Fully-Differential Amplifiers	Willy Sansen
1:30 - 3:00 pm	Bandgap Voltage References	Willy Sansen
3:30 -5:00 pm	Time-Assisted Analog Design	Pavan Hanumolu

THURSDAY, August 31

8:30 - 10:00 am	Noise Calculation and Simulation in SC & CT Circuits	Christian Enz
10:30 - 12:00 am	Noise and Offset Reduction Techniques	Christian Enz
1:30 - 5:00 pm	Matching Impairments in Mixed-Mode ICs	Herman Casier

FRIDAY, September 1

8:30 - 10:00 am	Modeling and Simulation of Mixed-Mode Circuits	Pavan Hanumolu
10:30 - 12:00 am	Interference Effects: CMRR/PSRR	Michiel Steyaert
1:30 - 3:00 pm	Design for EMC	Michiel Steyaert