MEAD Education S.A.

Transistor-Level Analog Design: Theory and Hands-on

EPFL, LAUSANNE, SWITZERLAND
JUNE 27 - JULY 1, 2016

MONDAY, JUNE 27

8:30 - 10:00 am	Introduction & MOS Transistors	Klaas Bult
10:30 - 12:00 am	Single-Stage OpAmps, Part 1	Klaas Bult
1:30 - 3:00 pm	Single-Stage OpAmps, Part 2	Klaas Bult
3:30 - 5:00 pm	Noise in MOS Transistors	Klaas Bult

TUESDAY, JUNE 28

8:30 - 10:00 am	Distortion	Klaas Bult
10:30 - 12:00 am	Basic Sub-Circuits	Klaas Bult
1:30 - 5:00 pm	Matching of MOS Transistors in Deep-Submicron	Marcel Pelgrom

WEDNESDAY, JUNE 29

8:30 - 10:00 am	Gain-Boosting & Settling Behavior	Klaas Bult
10:30 - 12:00 am	Two-Stage Amplifiers	Klaas Bult
1:30 - 5:00 pm	Layout Considerations in Mixed-Signal Circuit Design	Marcel Pelgrom

THURSDAY, JUNE 30

8:30 - 10:00 am	MOS Device Sizing	Maher Kayal
10:30 - 12:00 am	OTAs Procedural Sizing	Maher Kayal
1:30 - 5:00 pm	LAB SESSION: Basic OTA Design	M.Kayal + Assistants

FRIDAY, JULY 1

8:30 - 10:00 am	Digtally-Assisted Offset Compensation	Maher Kayal
10:30 - 12:00 am	LAB SESSION: Folded Cascode Design	M.Kayal + Assistants
1:30 - 3:00 pm	LAB SESSION: Offset Reduction Design	M.Kayal + Assistants